In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-12. (Cancelled)

13. (Original): An apparatus for binary number conversion, provided in a digital data processing system to convert an m-bit first binary number to a n-bit second binary number, wherein $n=m*q+r$, $0 \leqq r<m$, and m、n、q、r are positive integers, the apparatus for binary number conversion comprising:

a determination unit, input the first binary number, m, and n from an input port, and calculating q and r;

a bits replicator, receiving the first binary number, and q from the determination unit, and duplicating the first binary number q times to obtain a first number;

a mask, receiving the first binary number, m and r from the determination unit, and masking the least significant (m-r) bits of the first binary number to obtain a second number;

a bits swapper, receiving the first binary number from the determination unit, and swapping the second number of the first binary number and a third number formed by the significant (m-r) bits of the first binary number to obtain a third binary number;

an adder, receiving the third binary number from the bits swapper, and receiving the first binary number from the determination unit, then subtracting a value of the first binary number from a value of the third binary number to obtain a difference value;

a 2-level comparator, receiving the difference value from the adder, and generating a modification instruction based on a rule referring the difference value;

an incrementor/decrementor, receiving the second number from the mask, and receiving the modification instruction from the 2-level comparator, then modifying the second number according to the modification instruction to obtain a fourth number; and

a combine unit, receiving the first number from the bits replicator, and receiving the fourth number from the incrementor/decrementor, then making the first number and the fourth number respectively be most significant bits and least significant bits of the second binary number.

14. (Original): The apparatus of claim 13, wherein the digital data processing system is a video card.

15. (Original): The apparatus of claim 14, wherein the second binary number is a digital signal for representing colors.

16. (Original): The apparatus of claim 14, wherein the second binary number is a digital signal for representing coordinates.

17. (Original): The apparatus of claim 13, wherein the rule is:

when the difference value is larger than or equal to $0.5*(2^m-1)$, generating the modification instruction to order the incrementor/decrementor to add one to the second number to obtain the fourth number;

when the difference value is less than $-0.5*(2^m-1)$, generating the modification instruction to order the incrementor/decrementor to subtract one from the second number to obtain the fourth number and

when the difference value is not larger than or not equal to $0.5*(2^m-1)$, and not less than $-0.5*(2^m-1)$, generating the modification instruction to order the incrementor/decrementor not to modify the second number, and the second number is equal to the fourth number.